BNC

INSTRUCTION
MANUAL

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BNC

Pulse Generator
Model 8010

INSTRUCTION MANUAL

BERKELEY NUCLEONICS CORPORATION
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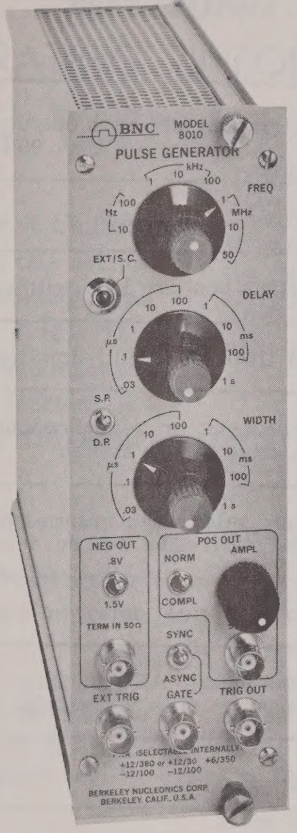
Warranty

Berkeley Nucleonics Corporation warrants all instruments, including component parts, to be free from defects in material and workmanship, under normal use and service for a period of one year. If repairs are required during the warranty period, contact the factory for component replacement or shipping instructions. Include serial number of the instrument. This warranty is void if the unit is repaired or altered by others than those authorized by the Berkeley Nucleonics Corporation.


BNC
MODEL 8010
PULSE GENERATOR
FREQ
DELAY
WIDTH
EXT/S.C.
S.P.
D.P.
NEG OUT
.8V
1.5V
TERM IN 50Ω
POS OUT
NORM
COMPL
AMPL
SYNC
ASYNC
EXT TRIG
GATE
TRIG OUT
BERKELEY NUCLEONICS CORP.
BERKELEY, CALIF., U.S.A.

SECTION 1
SPECIFICATIONS

FREQUENCY	a) 1 Hz to 50 MHz in 8 ranges, continuously adjustable. b) External trigger, 0 Hz to 50 MHz. c) Single cycle by front panel pushbutton.
DELAY	Less than 25 ns to 1 s in 9 ranges, continuously adjustable.
WIDTH	Less than 20 ns to 1 s in 9 ranges, continuously adjustable.
POSITIVE OUTPUT	a) Normal or complement; switch selectable. b) Amplitude: 500 mV to 5 V continuously adjustable into 50 Ω (TTL logic). c) Rise and fall times: 5 ns.
NEGATIVE OUTPUT	a) Amplitude: fixed -0.8 V pulse (NIM logic) into 50 Ω, or -1.5 V with base line offset of -0.5 V into 50 Ω (ECL logic); switch selectable. b) Rise and fall times: 3.5 ns.

. . . continued

DUTY FACTOR	Greater than 50% each output; in complementary pulse mode, duty factors larger than 90% may be attained.
TRIGGER OUT	Positive 1.1V square wave into 50 Ω.
EXTERNAL TRIGGER	Requires positive 1 V, with rate of rise greater than 3 V/ μs.
WAVEFORM DISTORTION	Less than 5% at full amplitude.
EXTERNAL GATE	Synchronous or asynchronous; switch selectable. Requires a positive 1.5 V signal.
SINGLE/DOUBLE PULSE	Switch selectable, minimum double pulse spacing of 20 ns. Pulse separation set by delay controls.
JITTER	Repetition rate, delay, or width, 0.1% +50 ps.
MECHANICAL	Double width AEC module, 2.70" wide by 8.70" high in accordance with TID-20893 (Rev. 3).
WEIGHT	3-1/2 lbs, net; 7 lbs, shipping.
POWER REQUIREMENTS	a) +12 V at 380 mA, -12 V at 100 mA, OR b) +12 V at 80 mA, -12 V at 100 mA, +6 V at 300 mA; Selectable internally. Easily changed by removing side cover and throwing slide switch into either position.

SECTION 2
OPERATING INFORMATION

2.1 INTRODUCTION

To aid in the understanding of the capabilities of the Model 8010 Pulse Generator, this section describes the operation of the controls and connectors present on the Model 8010. This instrument conforms electrically and mechanically to specifications for NIM (nuclear instrument modules) per AEC report TID-20893, Rev. 3.

2.2 FUNCTION OF CONTROLS & CONNECTORS

2.2.1 POWER CONNECTOR

Power is applied to the Model 8010 through this connector. Pin 34 is ground. Pin 16 is +12 V. Pin 17 is -12 V. Pin 10 is +6 V.

2.2.2 POWER SELECT

The Model 8010 may be operated from either ±12 V or ±12 V and +6 V supplies. With only ±12 V supplies, the power requirements are 380 mA for +12 V and 100 mA for -12 V. With ±12 V and +6 V supplies, the requirements are: 80 mA for +12 V, 100 mA for -12 V, and 300 mA for +6 V. The selection of this power option is accomplished by a slide switch mounted on the pc board. In order to operate this slide switch, the right-hand side cover must be removed.

2.2.3 FREQUENCY

This concentric switch and potentiometer combination provides the pulse repetition rate control. The switch selects one of eight internally generated repetition rate ranges or an EXT/S.C. range. With a vernier frequency control mounted concentrically to the range control, a continuous adjustment of the internal rep rate frequency from 1 Hz to 50 MHz is provided. In the EXT/S.C. range, only an EXTERNAL TRIGGER or the SINGLE CYCLE pushbutton will initiate a pulse cycle.

2.2.4 EXTERNAL TRIGGER AND SINGLE CYCLE

With the FREQ switch in the EXT/S.C. position, an EXTERNAL TRIGGER signal or SINGLE CYCLE pushbutton will start a pulse cycle. A single pulse cycle is initiated by the depression of the SINGLE CYCLE pushbutton on the front panel.

The Model 8010 can be externally triggered from 0 Hz to 50 MHz via signals at the EXT TRIG connector. Signals should be at least +1 V, with a rate of rise less than 3 V/μs. The input impedance at the EXT TRIG connector is 50 Ω.

2.2.5 GATE-SYNCHRONOUS/ASYNCHRONOUS

With proper signals into the EXT GATE connector, output and trigger signals can be gated on and off. A low level or short circuit at the EXT GATE connector results in no output or trigger pulses present at their respective connectors. An open circuit or a signal greater than +1.5 V at the EXT GATE connector results in the proper trigger and output pulses at their respective connectors.

The SYNC/ASYNC toggle determines whether the gated outputs and triggers will be synchronized with the gating waveform. In the SYNC mode, the internal clock is enabled by the gating signal. The output pulse train begins with the gate signal. For fixed width gate signals, a constant number of outputs will be gated on for a given internal frequency.

In ASYNC mode, the internal clock free runs and the signals from the clock are gated. Thus, the beginning of the gate may occur before, during, or after the occurrence of an output pulse.

Gate signals will gate SINGLE CYCLE, internal FREQUENCY, and EXTERNAL TRIGGER signals. The gate will operate in ASYNC mode on any of these trigger sources. In SYNC mode, the gate will operate on SINGLE CYCLE or internal FREQUENCY signals.

2.2.6 TRIG OUT

This connector provides a trigger signal to which pulse delays are referenced. The 50% point of the positive sloped edge is the zero delay point. The trigger level is about +1 V into 50 Ω. The TRIGGER OUT circuitry is a current source of about 20 mA that will saturate into high impedances at a level of about +4.5 V. A 50 Ω load should be used when working with narrow delays. With an internal clock, the output is a square wave. In the EXT/S.C. mode, if an EXTERNAL TRIGGER is applied, the TRIGGER OUT follows the EXTERNAL TRIGGER width; if the S.C. pushbutton is pressed, the TRIGGER OUT is 70 ns wide.

2.2.7 DELAY

This concentric switch/potentiometer control determines the delay between the leading edge of the trigger signal and the leading edge of the output pulse. Together with the nine coarse ranges, the vernier control provides for continuous adjustment of delays from 25 ns to 1 s.

2.2.8 WIDTH

This concentric switch/potentiometer combination controls the width of both output pulses. The output pulse begins at the end of the delay time and ends after a time determined by the WIDTH controls. The nine coarse ranges, together with the vernier control, provide for a continuous width adjustment from 20 ns to 1 s.

2.2.9 SINGLE PULSE / DOUBLE PULSE

The S.P. / D.P. toggle switch selects single pulse or double pulse operation. In the SINGLE PULSE mode, the output pulse starts after the DELAY time and lasts for a duration determined by the WIDTH controls.

In the DOUBLE PULSE mode, two pulses occur: one starts at essentially zero delay (at the positive slope of the trigger signal) and lasts for a duration set by the WIDTH controls; the other pulse occurs after the delay time for a duration set by the WIDTH controls. In the DOUBLE PULSE mode, the spacing between the two pulses is determined by the DELAY setting, and the width of both pulses is determined by the WIDTH controls. In the DOUBLE PULSE mode, both the width and the delay should be at least 20 ns for proper operation.

2.2.10 NEG OUT

The .8 V/1.5 V toggle switch allows the selection of one of two forms of negative outputs. With the toggle switch at .8 V, a fixed -0.8 V pulse into 50 Ω from a 0 V base line is selected. This is the standard fast NIM logic.

With the toggle switch in the 1.5 V position, ECL compatible logic levels into 50 Ω are available. The base line is -0.5 V, and the pulse top is -1.5 V.

2.2.11 POS OUT

The positive output connector and controls provide an adjustable positive output level with NORMAL or COMPLEMENTARY pulse operation. An AMPLITUDE control allows the pulse top level to vary from +0.5 V to +5 V. The AMPLITUDE control is an attenuator that should operate into 50 Ω in order to provide the 10:1 amplitude control.

A NORM/COMPL toggle switch provides either NORMAL or COMPLEMENTARY pulse operation. In the NORMAL pulse mode, the output pulse is at a high level for the duration of the pulse width and has a base line of about 0 V. In the COMPLEMENTARY mode, the pulse is near 0 V for the duration of the pulse width and at the adjustable high level at all other times. In the COMPLEMENTARY mode, duty factors larger than 90% can be obtained.

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section of the manual contains the description of the circuitry in the Model 8010 Pulse Generator. A complete block diagram, located in Section 5 of this manual, shows the overall relationships of the various circuits. A description of the block diagram is given below in paragraph 3.2. Detailed circuit description is given later in paragraph 3.3.

3.2 BLOCK DIAGRAM

3.2.1 GENERAL

The timing relationships of the Model 8010 are determined by the trigger sources, a delay one-shot and a width one-shot. A trigger source, which may be the internal frequency oscillator, an external trigger, or the single cycle pushbutton, triggers the delay one-shot. After the delay has been completed, the width one-shot period starts to mark the beginning of the pulse; the end of the width one-shot period marks the end of the pulse. The output from the width one-shot is amplified by positive and negative amplifiers and presented at the respective output connectors.

3.2.2 FREQUENCY OSCILLATOR

The Frequency Oscillator provides the internal clock pulses that initiate pulse cycles. The frequency range and vernier controls determine the frequency of this internal clock. In the EXT/S. C. range, the Frequency Oscillator is disabled and acts as an amplifier for pulses from the SINGLE CYCLE pushbutton. In the SYNCHRONOUS GATE mode, the Frequency Oscillator is enabled by the gate signals.

3.2.3 FREQUENCY AMPLIFIER

The Frequency Amplifier acts as an amplifier for signals from the Frequency Oscillator and accepts signals from the External Trigger Buffer. The signals from the Frequency Oscillator and the External Trigger Buffer are OR'ed at the Frequency Amplifier and presented to the Trigger Amplifier. In the ASYNCHRONOUS GATE mode, a gate input allows signals to leave the Frequency Amplifier.

3.2.4 GATE BUFFER

The Gate Buffer amplifies the signals from the EXT GATE connector and presents them to either the Frequency Oscillator or the Frequency Amplifier. The SYNC/ASYNC toggle switch determines whether the Frequency Amplifier or the Frequency Oscillator receives the signal from the Gate Buffer. A gate signal into either the Frequency Oscillator or Frequency Amplifier allows signals to leave that particular block.

3.2.5 EXTERNAL TRIGGER BUFFER

The External Trigger Buffer amplifies signals from the EXT TRIG connector and transmits the signal to the Frequency Amplifier.

3.2.6 TRIGGER AMPLIFIER

The Trigger Amplifier amplifies the signal from the Frequency Amplifier and presents it at the TRIG OUT connector. Another output from the Trigger Amplifier triggers the Delay One-Shot.

3.2.7 DELAY ONE-SHOT

The Delay One-Shot is a monostable multivibrator whose one-shot period is controlled by the DELAY range and vernier controls. The Delay One-Shot is triggered by the Trigger Amplifier to start the delay cycle. At the end of the Delay One-Shot period, the Double Pulse Circuitry is triggered.

3.2.8 DOUBLE PULSE CIRCUITRY

The Double Pulse Circuitry provides the triggering for the Width One-Shot. The D. P./S. P. toggle switch determines whether a signal marking the end of the Delay One-Shot period or signals marking both the beginning and end of the Delay One-Shot period are sent to the Width One-Shot.

3.2.9 WIDTH ONE-SHOT

The Width One-Shot is a monostable multivibrator whose one-shot period determines the WIDTH of the output pulse. The WIDTH range and vernier controls determine the length of the one-shot period. The output of the Width One-Shot then enters the Output Driver.

3.2.10 OUTPUT DRIVER

The Output Driver amplifies the signal from the Width One-Shot to drive both the Positive and Negative Amplifiers. This acts as a buffer stage between the Width One-Shot and the output amplifiers.

3.2.11 NEGATIVE AMPLIFIER

The output from the Output Driver is amplified by the negative amplifier, and the signal is presented at the NEG OUT connector. The .8 V / 1.5 V toggle selects whether the output levels will be NIM or ECL levels.

3.2.12 POSITIVE AMPLIFIER

The Positive Amplifier amplifies the signal from the Output Driver and presents a fixed amplitude signal to the Amplitude Control. The NORM / COMPL toggle switch determines whether the normal positive pulse signal or the complementary positive pulse signal enters the Amplitude Control.

3.2.13 AMPLITUDE CONTROL

The Amplitude Control attenuates the signal from the Positive Amplifier. This attenuator is designed to work into 50 Ω and presents a pulse at the POS OUT connector.

3.3 CIRCUIT DESCRIPTION

(Refer to Schematic 8010-1 in Section 5.)

3.3.1 FREQUENCY OSCILLATOR

IC1, a dual four-input ECL clock driver, forms an astable multivibrator that is the Frequency Oscillator. The multivibrator period is determined by a range capacitor and the position of fine frequency potentiometer, R5. The output of the multivibrator at Pin 13 of IC1 is sent to the Frequency Amplifier. Note that the ECL supplies are +5.2 V and ground. The positive supply level is established by the drop across R56 from the +6 V supply.

To understand the operation of the Frequency Oscillator, assume that Pin 6 has just gone high. This will cause Pin 8 to go low, forcing Pin 5 of IC1 lower. The voltage across the range capacitor cannot change instantaneously when Pin 8 of IC1 goes low. Pin 6 of IC1 is high and the range capacitor will charge positively through R2, R3 and R5. When Pin 5 is sufficiently positive to cause Pin 6 to go low, Pin 8 will go high causing Pin 5 to move even higher. The range capacitor now discharges negatively through R5. When Pin 5 is sufficiently low, Pin 6 will move high, and thus we begin another clock cycle.

In the EXT/S. C. range position, Pin 1 of IC1 is connected to Pin 3 of IC1 via R6. This connection forces the gates of IC1 into a stable state that is changed only during depression of the SINGLE CYCLE pushbutton. The stable state occurs as the high level at Pin 1 is fed back to Pin 3. This keeps the level at Pin 1 high until the SINGLE CYCLE pushbutton is depressed to force Pin 3 low. In the stable state Pin 6 is low, keeping Pin 8 high and Pin 13 low. Pin 5 is low since Pin 6 is low and no current can flow through feedback resistors R2, R3, and R5. When the SINGLE CYCLE pushbutton is depressed, Pin 3 is momentarily shorted to ground through C1 and Pin 6 is moved positively. This results in a momentarily positive pulse that is transmitted to the Frequency Amplifier. Pin 8 moves low to switch Pin 5 to a low level. Pin 5 starts to move positively as C3 is charged through R2, R3 and R5 from Pin 6. The gates revert back to their stable state. C1, which received some of the charge from C9 during depressing of the SINGLE CYCLE pushbutton, now discharges through R1, and the gates are ready for another single cycle.

With Pin 10 of IC1 low, the Frequency Oscillator operates properly as a single cycle amplifier or an astable multivibrator. The low level at Pin 10 has no control on the outputs at Pin 13 and Pin 8.

However, if Pin 10 were high, IC1 would cease to function as an astable multivibrator or a single cycle amplifier because Pin 13 would always be high and Pin 8 always low. We shall later see that the Gate Buffer, in SYNCHRONOUS mode, starts and stops the operation of the Frequency Oscillator at Pin 10.

3.3.2 FREQUENCY AMPLIFIER, GATE BUFFER, AND EXTERNAL TRIGGER BUFFER

There are three inputs into the Frequency Amplifier, one of the ECL gates in IC2. The inputs come from the Frequency Oscillator, the External Trigger Buffer, and the Gate Buffer. With the signals from the External Trigger Buffer and the Gate Buffer both low, the output of the Frequency Amplifier at Pins 6 and 1 are controlled by the Frequency Oscillator.

In the EXT/S. C. range, Pin 2 of IC2 is held at a high level by Pin 1 of IC1 via R8. With a low level or open circuit at the EXT TRIG connector, Q4, part of the External Trigger Buffer, remains off. D4 clamps the emitter of Q4 at approximately 300 mV below ground, and an open circuit or low level at the EXT TRIG connector is not sufficient to turn on Q4. Hence, Pin 2 of IC2 remains at a high level, keeping Pin 1 of IC2 high and Pin 6 of IC2 low. When a positive-going waveform turns on Q4, Pin 2 of IC2 will move low causing Pin 6 to move high and Pin 1 to move low. This state continues as long as the input signal keeps Q4 on. This output is transmitted to the Trigger Amplifier.

The Frequency Amplifier supplies signals to the Trigger Amplifier only when Pin 5 of IC2 is low. Pin 5 receives the signal from the Gate Buffer. In the ASYNC gate mode, if Pin 5 were high, the inputs at Pins 3 and 2 of IC2 have no effect on the outputs at Pins 6 and 1, and no signals are transmitted to the Trigger Amplifier.

With a high level or open circuit at the EXT GATE connector, Q3, the Gate Buffer is saturated resulting in a low level at its collector. This low level is transmitted via the SYNC/ ASYNC toggle switch to either the Frequency Oscillator or the Frequency Amplifier. In both cases the low level allows the Frequency Oscillator or the Frequency Amplifier to operate properly. If a low level is present at the EXT GATE connector, D1 conducts most of the current from R10 to keep Q3 off. This results in a high level at the collector of Q3 to disable either the Frequency Oscillator or the Frequency Amplifier. D2 clamps the emitter of Q3 at a diode drop below ground.

3.3.3 TRIGGER AMPLIFIER

When Pin 6 of IC2 moves high and Pin 1 of IC2 moves low, the Trigger Amplifier, Q5 and Q6, triggers the Delay One-Shot and presents a signal at the TRIG OUT connector. Q5 and Q6 is an emitter-coupled current mode pair. With Pin 1 of IC2 moving low and Pin 6 of IC2 moving high, Q5 is turned off and Q6 turned on. This results in a positive-going pulse at the collector of Q6 and a negative-going pulse at the collector of Q5. The transitions at the collector of Q5 are differentiated by L1 and R22 with only the negative spikes being transmitted by D8. Note that, in order to effect the required transitions at the inputs of the Trigger Amplifier, the Single Cycle circuit must recover to its stable state.

3.3.4 DELAY ONE-SHOT

The Delay One-Shot is comprised of Q8 and Q7. The stable state is with both Q7 and Q8 on, each supplying base current to the other. The negative-going pulse from the Trigger Amplifier to the base of Q8 will turn Q8 off. As Q8 turns off, Q7 will turn off, increasing the turn-off rate for Q8. The base of Q7 is now at a level determined by R61, the Delay vernier control. When one of the range capacitors, C12 through C19, charges sufficiently positive through R24 such that the emitter of Q7 is approximately one diode drop above its base, Q7 will start to turn on. This turns on Q8, which in turn turns Q7 on harder, and the one-shot reverts back to its stable state. As Q7 turns on, the range capacitor is discharged through D5 and R23. D6 prevents Q7 from saturating in the stable state. The output of the Delay One-Shot is a positive pulse at the collector of Q8 for the duration of the one-shot period.

3.3.5 DOUBLE PULSE CIRCUITRY

The Double Pulse Circuitry consists of part of IC2, Q9, Q10 and Q11. The signal at the collector of Q8 is converted into a differential signal by IC2, which drives emitter-coupled current mode pair, Q9, Q10. For the duration of the Delay One-Shot period, Q10 is on and Q9 is off. At the end of the Delay One-Shot period, Q10 turns off resulting in a negative pulse at its collector. This is transferred via D9 to the input of the Width One-Shot.

In the SINGLE PULSE mode, the signal at the collector of Q9 has no effect on the Width One-Shot, since Q11 is held off through the S.P./D.P. toggle switch.

In the DOUBLE PULSE mode, Q11 is turned on so that a negative-going spike at the collector of Q11 is transmitted via D10 to the Width One-Shot. With Q11 saturated, the collector of Q11 will move negatively only when the emitter of Q11 moves negatively. This occurs at the start of the Delay One-Shot when Q9 turns off.

Thus, in DOUBLE PULSE mode, negative spikes are transmitted to the Width One-Shot at the beginning of the Delay One-Shot period and at the end of the Delay One-Shot period. In the SINGLE PULSE mode, a negative spike is transmitted to the Width One-Shot only after the Delay One-Shot period.

3.3.6 WIDTH ONE-SHOT

The Width One-Shot functions in the same manner as did the Delay One-Shot. Again, a positive pulse at the output of the Width One-Shot, the collector of Q13, denotes the Width One-Shot period.

3.3.7 OUTPUT DRIVER

The Output Driver is an emitter-coupled current mode pair, Q14 and Q15, that is driven single-endedly by the signal from the Width One-Shot. Threshold is determined by the resistive voltage divider at the base of Q15. During the Width One-Shot period, Q14 turns on and Q15 off. L6 and L7 serve as peaking inductors to decrease the transition times at the outputs. The signals at the collectors of Q14 and Q15 are then transmitted to the Positive and Negative Amplifiers.

3.3.8 POSITIVE AMPLIFIER

The Positive Amplifier consists of Q16A, Q16B, Q17A and Q17B. The positive-going signal at the collector of Q15 is buffered by emitter followers Q16A and Q16B, connected in parallel, and sent to the Amplitude Control when the COMPL/NORM toggle switch is in the NORM position. The negative-going signal at the collector of Q14 is buffered by emitter followers Q17A and Q17B and is sent to the Amplitude Control when the toggle switch is in the COMPL position. The signal that is not sent to the Amplitude Control is loaded by R16 to provide a constant current drain from the +6 V supply.

3.3.9 AMPLITUDE CONTROL

The signal from the Positive Amplifier enters the Amplitude Control via the COMP/NORM toggle switch. The Amplitude Control is a bridged-T attenuator designed to operate into a 50 Ω load. In the maximum amplitude position, the signal from the selected paralleled emitter followers is transmitted directly to the POS OUT connector via a shorted R55. In the minimum amplitude position, the signal from the selected emitter followers is attenuated by R55 in series with the parallel equivalence of R54 and the load.

3.3.10 NEGATIVE AMPLIFIER

The Negative Amplifier consists of Q18 through Q20. Q20 is an emitter follower that drives the base of Q18, part of an emitter-coupled current mode pair. The other half of that pair, Q19, drives the load at the NEG OUT connector. The negative - going signal at the collector of Q14 causes Q18 to turn on and Q19 off. When Q19 turns off, the output level is determined by a resistor divider formed by the load, R51, and a resistor selected by the .8 V / 1.5 V toggle switch. When Q19 turns on, the current from the collector of Q19 is such that the output returns to the desired base line level.

3.3.11 POWER

A -6 V supply is formed by series diode, D15, from the -12 V supply. When the POWER SELECT slide switch is in the ±12 V position, R70 is placed in series with a +12 V supply. The drop across R70 from the +12 V supply forms the +6 V supply. The bulk of the current supplied by the +6 V supply is constant through the use of current mode pairs and constant output load conditions. When a +6 V supply is provided externally, R70 is switched out of the circuit.

SECTION 4
MAINTENANCE

4.1 GENERAL

This section of the manual contains calibration and trouble-shooting information. The Model 8010 requires little maintenance and calibration is minimal.

4.2 CALIBRATION

There are five internal adjustments in the Model 8010. Three of these adjustments are concerned with the frequency oscillator; the other two with the output pulse.

The Frequency Oscillator adjustment consists of C32, C33 and R3.

R3 and C32 are adjusted so that, in the 50 MHz range, the FREQ potentiometer in the MAX position causes the FREQ to just exceed 50 MHz.

Adjust C33 so that there is overlap from the 10 MHz range into the two adjacent ranges. Readjust R3 if necessary.

The remaining adjustments are concerned with the output waveform. Adjust R46 so that the negative output has a 0 V base line into 50 Ω in the .8 V (NIM) switch position.

R68 adjusts the amount of drive to the output amplifiers. Increasing the drive decreases the transition times, but increases the waveform distortion. Too little drive results in transition times that are too slow. R68 is adjusted to obtain the best compromise between waveform distortion and transition time speed. Do not allow the base line of the positive pulse to move above ground.

4.3 TROUBLE-SHOOTING

A thorough understanding of the block diagram aids in isolating the area of the trouble. By probing at the inputs and outputs of the various blocks, the area of trouble is quickly located. Start from the faulty block.

SECTION 5

- PARTS LIST AND SCHEMATICS -

ABBREVIATIONS

CER	CERAMIC	UH	MICROHENRY
COMP	COMPOSITION	UF	MICROFARAD
ELEC	ELECTROLYTIC	PF	PICOFARAD
MIC	MICA	TAN	TANTALUM
K	KILOHM	V	WORKING VOLTS
M	MEGOHM	VAR	VARIABLE
MF	METAL FILM	W	WATTS

--------------------NOTE--------------------

The number in the second column is the BERKELEY NUCLEONICS re-order number

PC BOARD 8010B-1 649-080

C1	110-014	0.01UF 1KV GMV CER
C2	120-012	350 UF 16V ELEC
C3	122-015	33UF 10% 25V TAN
C4	122-003	3.3 UF 10% 15V TAN
C5	122-008	0.33 UF 10% 35V TAN
C6	114-004	0.033UF 10% 600V MYL
C7	114-005	0.0033UF 10% 600V MYL
C8	110-003	25PF 10% 1KV CER
C9	110-014	0.01UF 1KV GMV CER
C10		NOT USED
C11	110-016	0.47UF +80-20% 16V CER
C12	120-012	350UF +50-10% 16V ELEC
C13	120-007	100UF +50 -10% 16V ELEC
C14	120-011	10UF +50 -10% 25V ELEC
C15	120-010	1 UF +50 -10% 50V ELEC
C16	114-020	0.1UF 10% 100V MYL
C17	114-025	0.01UF 10% 200V MYL
C18	114-001	0.001UF 10% 600V MYL
C19	112-004	100PF 5% 500V MIC
C20	112-014	680PF 5% 500V MIC
C21	120-012	350UF +50 -10% 16V ELEC
C22	120-007	100UF +50 -10% 16V ELEC
C23	120-011	10UF +50 -10% 25V ELEC
C24	120-010	1UF +50 -10% 50V ELEC
C25	114-020	0.1UF 10% 100V MYL
C26	114-025	0.01UF 10% 200V MYL
C27	114-001	0.001UF 10% 600V MYL
C28	122-004	100PF 10% 35V MIC
C29	110-014	0.01UF 1KV GMV CER
C30	112-002	33PF 5% 500V MIC
C31	112-013	470PF 5% 500V MIC
C32	130-001	2.7-20PF VAR CER (TRIMMER)
C33	130-003	45-50PF VAR CER (TRIMMER)
C34	112-014	680PF 5% 500V MIC
C35	110-019	0.05UF 20% 25V CER
C36	110-014	0.01UF GMV 1KV CER
C37	110-003	25PF 10% 1KV CER
C38	110-004	33PF 10% 1KV CER
C39	112-006	180PF 10% 1KV MIC
C40	110-014	0.01UF GMV 1KV CER
C41	110-016	0.47UF +80-10% 10V CER
C42	120-007	100UF 10% 1KV ELEC
C43	122-015	33UF 10% 25V TAN
C44	122-015	33UF 10% 25V TAN

C45	122-015	33UF 10% 25V TAN
C46	110-003	25PF 10% 1KV CER

D1	411-004	1N4152
D2	411-002	1N270
D3	411-004	1N4153
D4	411-002	1N270
D5	411-002	1N270
D6	411-004	1N4152
D7	411-002	1N270
D8	411-004	1N4152
D9	411-004	1N4152
D10	411-004	1N4152
D11	411-002	1N270
D12	411-002	1N270
D13	411-004	1N4152
D14	411-004	1N4152
D15	412-010	1N5234B
D16	411-004	1N4152
D17	411-004	1N4152

L1	310-003	1UH
L2	310-002	0.47UH
L3	310-002	0.47UH
L4	310-011	0.33UH
L5	310-001	0.15UH
L6	310-012	0.68UH
L7	310-002	0.47UH
L8		SEE SCHEMATIC
L9		SEE SCHEMATIC
L10	310-013	0.22UH
L11	310-011	0.33UH

Q3	430-007	2N2369
Q4	430-007	2N2369
Q5	430-026	MPS3640
Q6	430-026	MPS3640
Q7	430-026	MPS3640
Q8	430-007	2N2369
Q9	430-026	MPS3640
Q10	430-026	MPS3640
Q11	430-007	2N2369
Q12	430-026	MPS3640
Q13	430-007	2N2369
Q14	430-007	2N2369
Q15	430-007	2N2369
Q16A	430-007	2N2369
Q16B	430-007	2N2369
Q17A	430-007	2N2369
Q17B	430-007	2N2369
Q18	430-026	MPS3640
Q19	430-026	MPS3640
Q20	430-026	MPS3640

R1	212-104	100K 5% 1/2W COMP
R2	212-470	47 5% 1/2W COMP
R3	244-021	100 5% VAR
R4		NOT USED
R5		2K (SEE S2) VAR
R6	212-560	561 5% 1/2W COMP
R7	212-331	330 5% 1/2W COMP
R8	212-221	220 5% 1/2W COMP
R9	212-222	2.2K 5% 1/2W COMP
R10	212-471	470 5% 1/2W COMP
R11	212-222	220 5% 1/2W COMP
R12	212-182	1.8K 5% 1/2W COMP
R13	212-102	1K 5% 1/2W COMP
R14	212-221	220 5% 1/2W COMP
R15	212-222	2.2K 5% 1/2W COMP
R16	212-122	1.2K 5% 1/2W COMP
R17	212-560	56 5% 1/2W COMP
R18	212-101	100 5% 1/2W COMP
R19	212-682	6.8K 5% 1/2W COMP
R20	212-331	330 5% 1/2W COMP
R21		NOT USED
R22	212-431	430 5% 1/2W COMP
R23	212-270	27 5% 1/2W COMP
R24	212-222	2.2K 5% 1/2W COMP
R25	212-391	390 5% 1/2W COMP

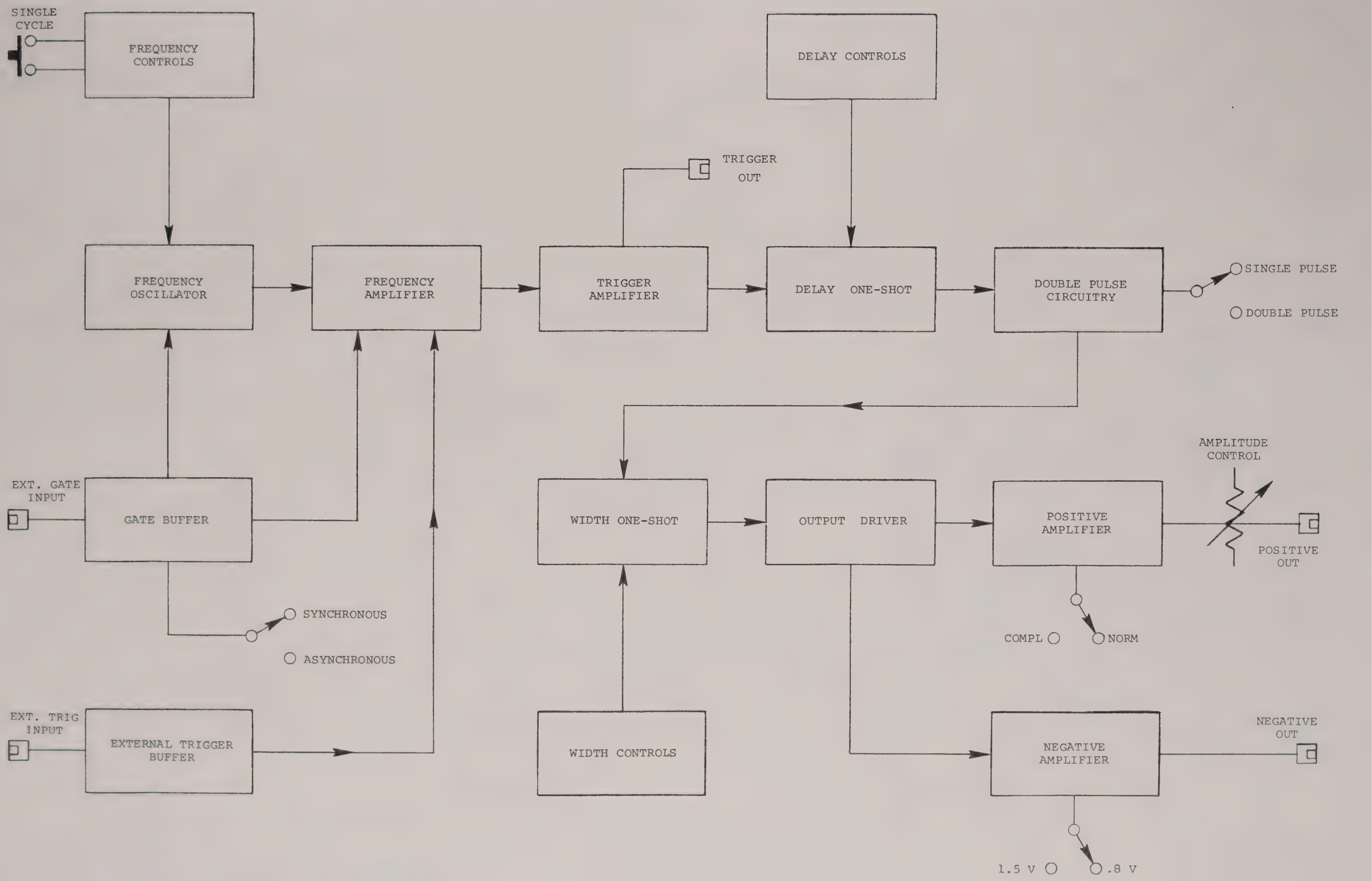
R26	212-222	2.2K 5% 1/2W COMP
R27	212-331	330 5% 1/2W COMP
R28	212-332	3.3K 5% 1/2W COMP
R29	212-271	270 5% 1/2W COMP
R30	212-271	270 5% 1/2W COMP
R31	212-220	22 5% 1/2W COMP
R32	212-222	2.2K 5% 1/2W COMP
R33	212-222	2.2K 5% 1/2W COMP
R34	212-221	220 5% 1/2W COMP
R35	212-221	220 5% 1/2W COMP
R36	212-182	1.8K 5% 1/2W COMP
R37	212-391	390 5% 1/2W COMP
R38	212-122	1.2K 5% 1/2W COMP
R39	212-302	3K 5% 1/2W COMP
R40	212-221	220 5% 1/2W COMP
R41	212-221	220 5% 1/2W COMP
R42	212-221	220 5% 1/2W COMP
R43	212-392	3.9K 5% 1/2W COMP
R44	212-102	1K 5% 1/2W COMP
R45	212-122	1.2K 5% 1/2W COMP
R46	244-022	200 1/4W VAR SINGLE TURN
R47	212-820	82 5% 1/2W COMP
R48	212-102	1K 5% 1/2W COMP
R49	212-560	56 5% 1/2W COMP
R50	212-391	390 5% 1/2W COMP
R51	212-151	150 5% 1/2W COMP
R52		NOT USED
R53	211-510	51 5% 1W COMP
R54	212-510	51 5% 1/2 W COMP
R55	240-009	50 T-PAD SINGLE TURN
R56	222-060	10 10% 1/4W MF
R57	222-060	10 10% 1/4W MF
R58	212-222	2.2K 5% 1/2W COMP
R59	212-271	270 5% 1/2W COMP
R60	212-181	180 5% 1/2W COMP
R61		2K (SEE S4)
R62		2K (SEE S6)
R63	212-222	2.2K 5%1/2W COMP
R64	212-271	270 5% 1/2W COMP
R65	212-181	180 5% 1/2W COMP

R66	212-510	51 5% 1W COMP
R67	212-222	2.2K 5% 1/2W COMP
R68	244--022	200 VAR SINGLE TURN
R69	212-471	470 5% 1/2W COMP
R70	231-003	18 1% 5W WIRE WOUND
R71	212-510	51 5% 1/2W COMP
R72	212-200	20 5% 1/2W COMP
R73	212-270	27 5% 1/2W COMP
R74	212-270	27 5% 1/2W COMP
R75	212-270	27 5% 1/2W COMP
R76	212-270	27 5% 1/2W COMP
R77	212-330	33 5% 1/4W COMP
R78	213-330	33 5% 1/4W COMP
R79	212-011	910 5% 1/2W COMP
R80	212-331	330 5% 1/2W COMP
R81	213-510	51 5%1/2W COMP
R82	212-510	51 5%1/2W COMP
R83	213-330	33 5%1/4W COMP

S1	612-001	TOGGLE SWITCH
S2	610-019	ROTARY SWITCH WITH 2K VAR
S3	611-002	TOGGLE SWITCH
S4	610-019	ROTARY SWITCH WITH 2K VAR
S5	611-006	TOGGLE SWITCH
S6	610-019	ROTARY SWITCH WITH 2K VAR
S7	611-006	TOGGLE SWITCH
S8	611-002	TOGGLE SWITCH
S9	613-001	SLIDE SWITCH

ADAPTER BOARD 8010-4 649-065

C1	110-019	0.05UF 20% 25V CER
R1	223-013	560 X5 SIP
Z1	440-044	MC10105
	621-013	ELEVATED 16 PIN SOCKET

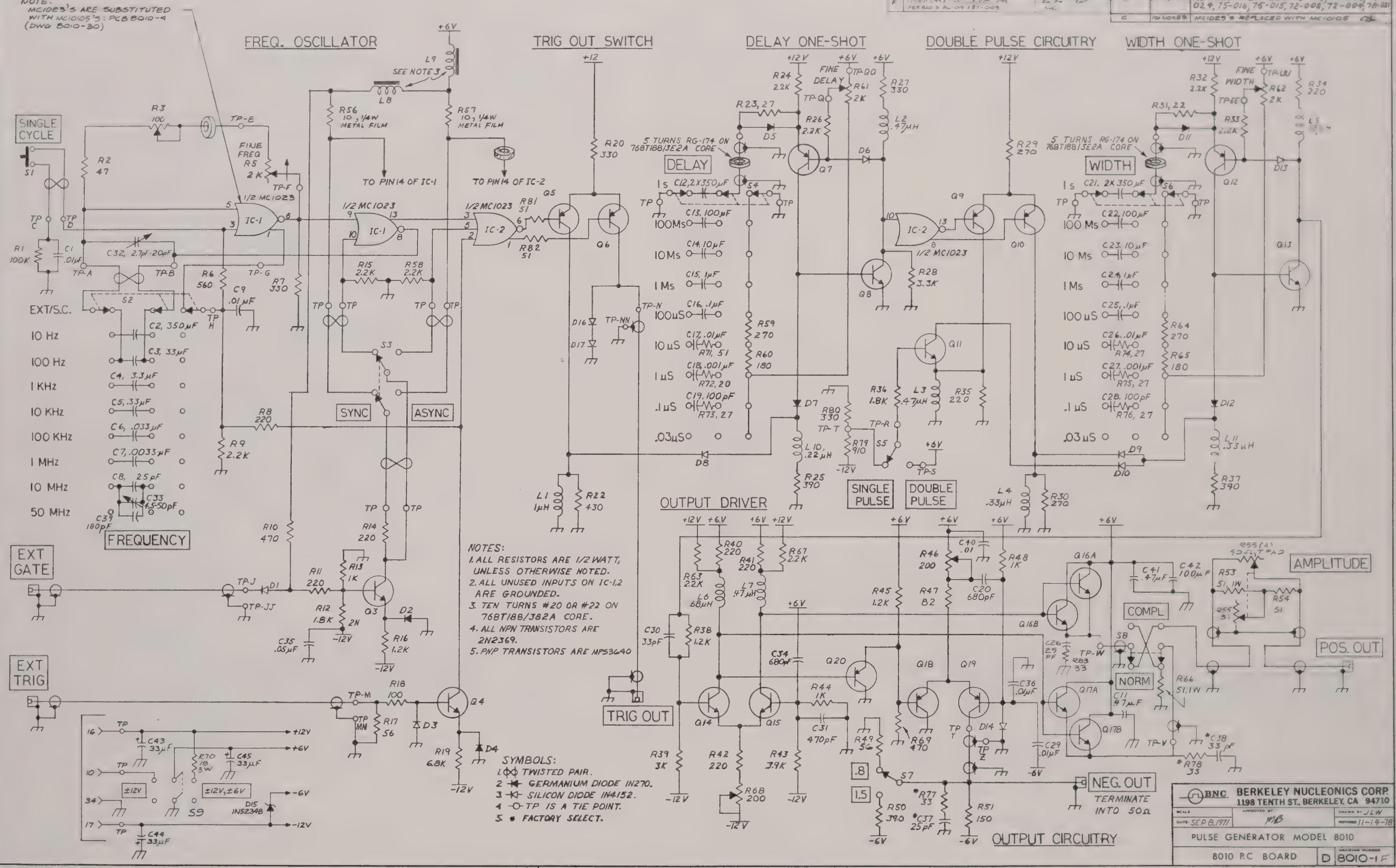

SINGLE CYCLE
FREQUENCY CONTROLS
DELAY CONTROLS
TRIGGER OUT
FREQUENCY OSCILLATOR
FREQUENCY AMPLIFIER
TRIGGER AMPLIFIER
DELAY ONE-SHOT
DOUBLE PULSE CIRCUITRY
SINGLE PULSE
DOUBLE PULSE
AMPLITUDE CONTROL
EXT. GATE INPUT
GATE BUFFER
WIDTH ONE-SHOT
OUTPUT DRIVER
POSITIVE AMPLIFIER
POSITIVE OUT
SYNCHRONOUS
ASYNCHRONOUS
COMPL
NORM
EXT. TRIG INPUT
EXTERNAL TRIGGER BUFFER
WIDTH CONTROLS
NEGATIVE AMPLIFIER
NEGATIVE OUT
1.5 V
.8 V

BLOCK DIAGRAM MODEL 8010

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	D	CHG'D R19: 1.2K→6.8K, R29: 270→330, R30: 360→270, PER ECO 84-035, ADDED C43—C45 PER ECO 85-005.	6-5-85	[illegible]
	E	CHG'D R56 & 57 FROM 10Ω, 1/2W, CC TO 10Ω, 1/4W, MF PER ECO 86-010	2/28/86	[illegible]
	F	ADDED C45 [illegible] PER ECO'S 86-019, 87-005	[illegible]	[illegible]

REV. LTR	DATE	REVISION
A	15 MAY 72	CHANGE: C7 TO .0033μF, C6 TO .033μF. C5 TO .33μF, C4 TO 3.3μF. C3 TO 33μF. C2 TO 350μF. ADD R79, 910Ω, & R80, 330Ω PER ECO 72-004
B	14 NOV 78	REVISED PER ECO 78-018, 77-003, 75-024, 75-016, 75-015, 72-008, 72-004, 78-021
C	16 NOV 83	MC1023'S REPLACED WITH MC10105

NOTE:
MC1023'S ARE SUBSTITUTED WITH MC10105'S: PCB 8010-4 (DWG 8010-30)


FREQ. OSCILLATOR
TRIG OUT SWITCH
DELAY ONE-SHOT
DOUBLE PULSE CIRCUITRY
WIDTH ONE-SHOT
OUTPUT DRIVER
OUTPUT CIRCUITRY
SINGLE CYCLE
S1
FINE FREQ R5 2K
R3 100
R2 47
R1 100K
C1 .01μF
C32 2.7pF-20pF
TP-A
TP-B
TP-C
TP-D
TP-E
TP-F
TP-G
TP-H
S2
EXT/S.C.
10 Hz
100 Hz
1 KHz
10 KHz
100 KHz
1 MHz
10 MHz
50 MHz
C2, 350μF
C3, 33μF
C4, 3.3μF
C5, .33μF
C6, .033μF
C7, .0033μF
C8, 25pF
C33 4.5-50pF
C39 180pF
FREQUENCY
R6 560
C9 .01μF
R7 330
R8 220
R9 2.2K
R10 470
1/2 MC1023
IC-1
IC-2
L8
L9
SEE NOTE 3
R56 10, 1/4W METAL FILM
R57 10, 1/4W METAL FILM
TO PIN 14 OF IC-1
TO PIN 14 OF IC-2
+6V
R15 2.2K
R58 2.2K
S3
SYNC
ASYNC
R81 51
R82 51
Q5
Q6
+12
R20 330
D16
D17
TP-N
TP-NN
L1 1μH
R22 430
D8
TRIG OUT
EXT GATE
TP-J
TP-JJ
D1
R11 220
R12 1.8K
R13 1K
2N
Q3
D2
R14 220
R16 1.2K
C35 .05μF
-12V
EXT TRIG
TP-M
TP-MM
R17 56
R18 100
D3
Q4
R19 6.8K
D4
16
10
34
17
C43 33μF
R70 18 3W
C45 33μF
±12V
±12V, ±6V
S9
D15 1N5234B
C44 33μF
+12V
-6V
5 TURNS RG-174 ON 76BT188/3E2A CORE
DELAY
1 s
100 Ms
10 Ms
1 Ms
100 μS
10 μS
1 μS
.1 μS
.03 μS
C12, 2×350μF
C13, 100μF
C14, 10μF
C15, 1μF
C16, .1μF
C17, .01μF
R71, 51
C18, .001μF
R72, 20
C19, 100pF
R73, 27
S4
R59 270
R60 180
R23, 27
D5
R24 2.2K
R26 2.2K
TP-Q
TP-QQ
FINE DELAY
R61 2K
Q7
D6
R27 330
L2 .47μH
Q8
R28 3.3K
D7
L10 .22μH
R25 390
R80 330
TP-T
R79 910
S5
TP-R
TP-S
SINGLE PULSE
DOUBLE PULSE
R36 1.8K
L3 .47μH
R35 220
Q11
Q9
Q10
R29 270
L4 .33μH
R30 270
WIDTH
C21, 2×350μF
C22, 100μF
C23, 10μF
C24, 1μF
C25, .1μF
C26, .01μF
R74, 27
C27, .001μF
R75, 27
C28, 100pF
R76, 27
S6
R64 270
R65 180
R31, 22
D11
R32 2.2K
R33 2.2K
TP-EE
TP-UU
FINE WIDTH
R62 2K
R34 220
L5
Q12
D13
Q13
D12
L11 .33μH
R37 390
D9
D10
R40 220
R41 220
R63 2.2K
R67 2.2K
L6 68μH
L7 .47μH
C30 33pF
R38 1.2K
C34 680pF
Q14
Q15
R39 3K
R42 220
R68 200
R43 3.9K
R44 1K
C31 470pF
Q20
R45 1.2K
R46 200
R47 82
C40 .01
C20 680pF
R48 1K
Q18
Q19
R49 56
R69 470
S7
.8
1.5
R50 390
R77 33
C37 25pF
R51 150
TP-Y
TP-Z
D14
C36 .01μF
C29 .01μF
Q16A
Q16B
Q17A
Q17B
C26 25 PF
R83 33
TP-W
C41 .47μF
C42 100μF
C11 .47μF
COMPL
NORM
S8
R66 51, 1W
TP-V
C38 33 pF
R78 33
AMPLITUDE
R55 (A) 50Ω T-PAD
R53 51, 1W
R54 51
R55 51
POS. OUT
NEG. OUT
TERMINATE INTO 50Ω

NOTES:
1. ALL RESISTORS ARE 1/2 WATT, UNLESS OTHERWISE NOTED.
2. ALL UNUSED INPUTS ON IC-1,2 ARE GROUNDED.
3. TEN TURNS #20 OR #22 ON 76BT188/3E2A CORE.
4. ALL NPN TRANSISTORS ARE 2N2369.
5. PNP TRANSISTORS ARE MPS3640

SYMBOLS:
1. ∞ TWISTED PAIR.
2. ◄ GERMANIUM DIODE 1N270.
3. ◄ SILICON DIODE 1N4152.
4. -○- TP IS A TIE POINT.
5. * FACTORY SELECT.

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

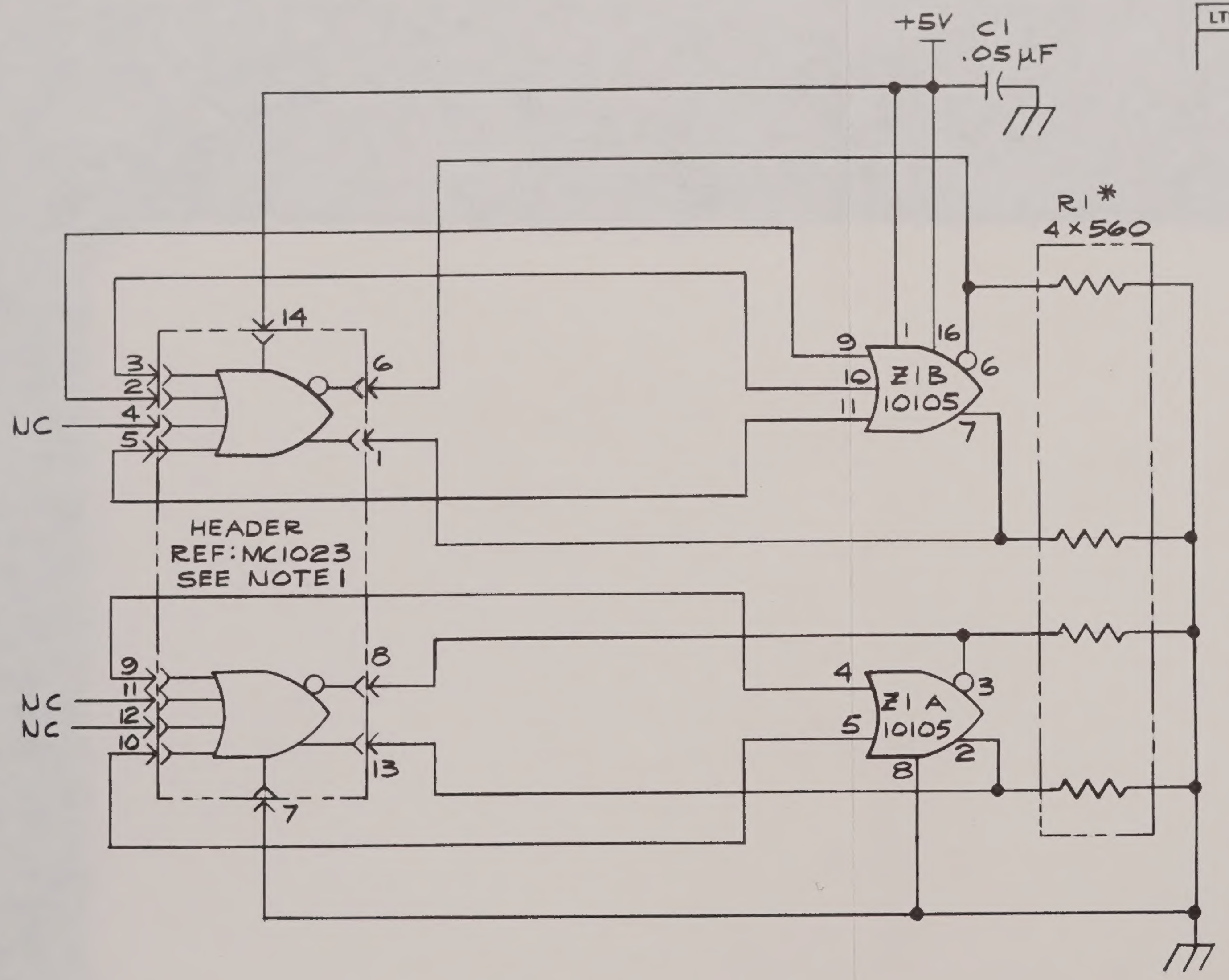
SCALE	APPROVED BY MB	DRAWN BY JLW
DATE: SEP 8, 1971		REVISED 11-14-78

PULSE GENERATOR MODEL 8010

8010 P.C BOARD | D | DRAWING NUMBER 8010-1F

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED


+5V
C1
.05µF
R1*
4×560
14
3
2
4
5
NC
6
1
HEADER
REF: MC1023
SEE NOTE 1
9
11
12
10
NC
NC
8
13
7
9
1
16
10
11
Z1B
10105
6
7
4
5
Z1A
10105
3
2
8

NOTES:

1. HEADER, 14 PIN BNC # 620-016 REPLACES IC MC1023.
2. * DENOTES RESISTOR NETWORK 4×560 Ω.

REF: PCB 8010-4

BNC **BERKELEY NUCLEONICS CORP.**
1198 TENTH ST., BERKELEY, CA 94710

SCALE ~	APPROVED BY EDK	DRAWN BY JWC
DATE 4-22-82		REVISED

PULSE GENERATOR: MODEL 8010

ADAPTOR BOARD

B DRAWING NUMBER 8010-30

KLINGLER K-VEL

94024